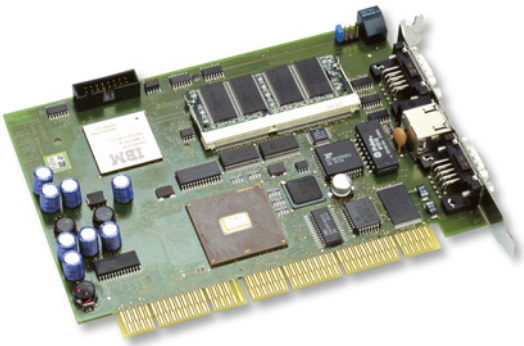
ELTEC systems

BAB 911

PowerPC 755 Based CompactPCI Board



MANUAL

Revision 1B

ELTEC systems

Revision

Revision	Changes	Date / Name
0A	First Edition	17.01.02 abr
1A	First Edition, valid for Hardware revision 1B	05.02.02 GM
1B	Disclaimer new	08.11.06 hh

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Federal communications commission statement

- This device complies with FCC Rules Part 15. Operation is subject to the following two conditions:
- This device may not cause harmful interference, and
- This device must accept any interference received including interference that may cause undesired operation.
- This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with

manufacturer's instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try correct the interference by one or more of the following measures:

- ↪ Reorient or relocate the receiving antenna.
- ↪ Increase the separation between the equipment and receiver.
- ↪ Connect the equipment to an outlet on a circuit different from that to which the receiver is connected.
- ↪ Consult the dealer or an experienced radio/TV technician for help.
- ↪ The us of shielded cables for connection of the monitor to the graphics card is required to assure compliance with FCC regulations. Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Canadian department of communications statement

- ↪ This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.
- ↪ This class B digital apparatus complies with Canadian ICES-003

SAFETY INFORMATION

Electrical safety

- ↪ To prevent electrical shock hazard, disconnect the power cable from the electrical outlet before reloading the system.

- When adding or removing devices to or from the system, ensure that the power cables for the devices are unplugged before the signal cables are connected. If possible, disconnect all power cables from the existing system before you add device.
- Before connecting or removing signals cables from motherboard, ensure that all power cables are unplugged.
- Make sure that your power supply is set to the correct voltage in your area. If you are not sure about the voltage of the electrical outlet you are using, contact your local power company.
- If the power supply is broken, do not try to fix it by yourself. Contact a qualified service technician or your retailer.

Operation safety

- Before installing the motherboard and adding devices on it, carefully read the manuals that came with the package.
- Before using the product, make sure all cables are correctly connected and the power cables are not damaged. If you detect any damage, contact your dealer immediately.
- To avoid short circuits, keep paper clips, screws, and staples away from connectors, slots sockets and circuitry.
- Avoid dust, humidity, and temperature extremes. Do not place the product in any area where it may become wet.
- Place the product on a stable surface.
- If you encounter technical problems with the product, contact a qualified service technician or your retailer.

EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

IMPROTANT INFORMATION

This product is not an end user product. It was developed and manufactured for further processing by trained personnel.

RECYCLING

Please recycle packaging environmentally friendly:
Packaging materials are recyclable. Please do not dispose packaging into domestic waste but recycle it.

Please recycle old or redundant devices environmentally friendly:
Old devices contain valuable recyclable materials that should be reutilized. Therefore please dispose old devices at collection points which are suitable.

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1 Specification

1.1 Main Features

- PowerPC-based PCISA CPU board
- PCI master interface
- CPU PowerPC 750CX(e) 400 MHz
- 256 KB on-chip L2-cache
- Up to 256 MByte SDRAM on SODIMM
- 10 / 100 Mbit/s network interface (10BaseT / 100BaseTX)
- Two serial channels
- 2 KB nvSRAM for storing application- / process-data
- PCISA (PISA) format with PCI interface for up to 4 slots
- OS-9 BSP support

1.2 Specification Details

The BAB 911 is a PowerPC-based single board computer with a PISA interface. The small format permits setting up small industrial realtime systems.

The board is based on the Motorola MPC 107 chip, the reference for PowerPC designs. Also, availability for longer periods than what is common in the PC market is guaranteed.

1.2.1 CPU Kernel

An up-to-date PowerPC CPU is supported: PowerPC 750CXe, compatible to the PowerPC 750 at 400 MHz. The CPU has FPU, MMU, first level cache (32KB each for instruction and data) and a L2 cache (256 KB unified) on the chip. It contains dual integer units, that can operate in parallel for certain instructions; the floating point unit is optimized for fast single precision multiply-add operations. Performance is characterized by the SPECint numbers of 17.4 and SPECfp 11.7.

1.2.2 Memory Configuration

The 64-bit wide memory allows configurations of up to 256 (512 when available) MByte with 100 MHz SDRAMs in a single SODIMM module. The implementation in SODIMM has been selected due to the smaller size and thus shorter signals, compared to standard DIMM modules. Memory size is detected automatically. The second-level cache, due to its location in the CPU itself, runs with the full CPU clock.

1.2.3 Chip set

The chip set, a Motorola MPC 107, contains the SDRAM memory controller, the interrupt controller, and the PCI host bridge for 32-bit/33-MHz PCI. Additionally, it has logic to access an 8-bit wide ROM, it has timers, a DMA controller, and it generates clocks.

1.2.4 Boot PROM

Boot code is stored in a Flash EPROM (size 512 KB) which enables easy code updates. The current boot proms contains self test code, PCI initialization routines, as well as OS boot code for OS-9 via Ethernet (BootP).

1.2.5 Ethernet Interface

The network interface uses the network controller i82559ER for 10/100 Mbit/s transfers with 10BaseT (twisted pair) or 100Base TX connectivity. Automatic speed detection is included. A Link LED and an Activity LED allow an easy check whether the Ethernet connection works.

1.2.6 Serial I/O

Two asynchronous 16550-compatible serial channels with up to 115 KBaud transfer rate and 16-byte FIFO with RS232 levels are available.

1.2.7 PISA Interface

The PISA interface is implemented with system slot capabilities for 32-bit PCI systems. It features transfer rates of up to 128 MByte/s between board-internal resources and PISA devices. The PISA interface uses only the PCI bus signals.

The board must occupy the PCI system slot and it will set up all PCI peripherals on the PCI back plane. The board can drive PCI buses (passive back planes) with up to 4 peripheral slots, all of them can obtain bus mastership (DMA).

1.2.8 Timer

The BAB 911 has four programmable timers, located in the MPC 107, for timing interrupts in the 1 µs to 1000 ms range. Three of these timers are intended for use with user-written drivers, they are not used by the operating system or the BSP, one may be used by the OS.

The additional CPU-internal decrementer is used for generating the OS ticker interrupt.

1.2.9 Non-volatile Memory

A non-volatile memory for storing system boot parameters (512 B) is mounted on the board, and additionally 2 KB user memory that is not used by ELTEC.

User memory is implemented in a non-volatile RAM using a combination of SRAM and EEPROM. The EEPROM is automatically programmed with SRAM data during power-down and supplies data to the SRAM during power-up. Data transfer rate is 5 MByte/s. Only byte-access is allowed.

1.2.10 Operating systems

The software support for the BAB 911 includes the board support package for OS-9 3.0.

1.2.11 On-board I/O

All on-board-I/O (2 * serial and 100BaseTx) is routed to the front panel.

1.2.12 Miscellaneous

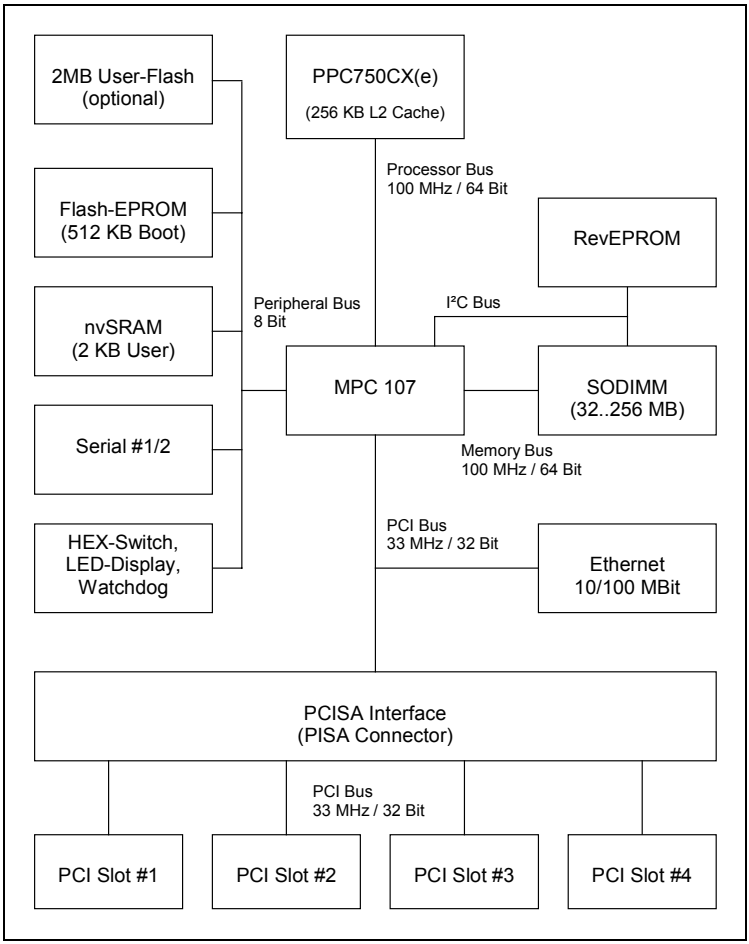
Due to the use of a PISA connector the number of external PCI slots is limited to 4. If more than 4 external slots are needed, a back plane with an integrated PCI-PCI bridge must be used.

1.2.13 Related Documents

IBM PowerPC 750CX/750CXe RISC Microprocessor User's Manual. This is the CPU manufacturer's description of the PowerPC itself and the assembly language command set.

Motorola MPC 107 PCI Bridge/Memory Controller User's Manual.

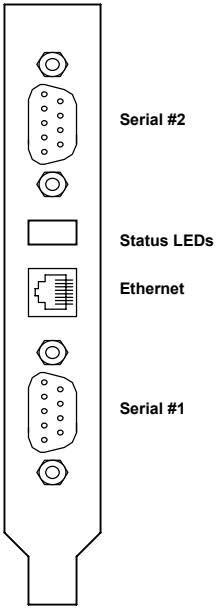
Figure 1—1: Block Diagram



2 Installation

2.1 BAB 911 I/O

Figure 2—1: Connection Diagram



2.1.1 What‘s needed for Installation

The BAB 911 must be installed into a PISA backplane. A terminal (or a PC with a terminal emulator program) connected to serial #1 and set to 9600 baud, 8 bit, no parity, is needed to check boot messages and to change boot settings. If the operating system is booted over Ethernet, a network connection is needed.

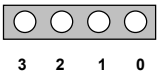
2.1.2 SODIMM Installation

The BAB 911 requires one 144-pin SODIMM SDRAM module, that supports CAS-latency 2 at 100 MHz, to be fitted into the SODIMM socket X701. These modules are currently available with a capacity of up to 256 Mbyte. In the near future there may also be 512 Mbyte modules that are supported by the BAB 911. The firmware reads the type and size of the SODIMM from the SPD (Serial Presence Detect) EEPROM installed on the memory module, and tests the module. If the test fails or the firmware reports the wrong size the module is not suitable for the BAB 911.

2.1.3 Status LEDs

There are four status LEDs on the front panel of the BAB 911. The LEDs are controlled by software.

Figure 2—2: LEDs



2.1.4 Ethernet Status LEDs

At the ethernet connector there are two LEDs indicating link status and network activity.

Figure 2—3: Ethernet Status LEDs

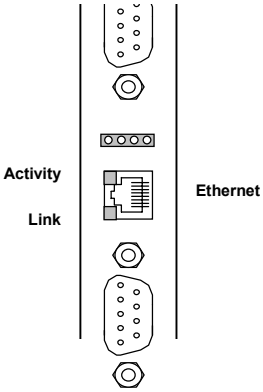


Table 2—1: Ethernet Status LEDs

LED	Color	Description
Activity	Green	Board power ok; network not initialized or no link pulses
	Yellow	Network activity
	off	Link pulses detected; no network activity
Link	Green	100 Mbit/s link pulses detected
	Yellow	10 Mbit/s link pulses detected
	Off	No link pulses detected

3 Connector Assignments

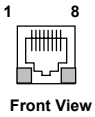
Please check the connector assignments before using any interface.

3.1 Front Panel Connectors

3.1.1 Ethernet Connector

Table 3—1: ETHERNET (8-pin Telephone Jack Connector)

Pin	Signal
1	TXD+
2	TXD-
3	RXD+
4	nc
5	nc
6	RXD-
7	nc
8	nc



Front View

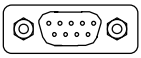
3.1.2 Serial Ports 1 and 2 Connectors

Table 3—2: COM1, COM2 (9-pin min-D Connector)

Pin	Signal
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

Front View

Pin 1



3.1.3 PISA Connector

Table 3—3: PISA Connector

Pin	ISA-Bus		PCIbus	
	top layer up row	bot layer up row	top layer low row	bot layer low row
1		GND	I2CLK	I2DAT
2			GND	GND
3		VCC	INTB#	INTA#
4			INTD#	INTC#
5			VCC	VCC
6				
7		-12V	VCC	VI/O
8			PCIRST#	PCICLK2
9		+12V	GNT#0	GND
10		GND	REQ#0	GNT#1
11			GND	GND
12			PCICLK1	REQ#1
13			GND	AD31
14			AD30	AD29
15			REQ#2	PCICLK3
16				
17			GNT#2	PCICLK4
18			AD28	AD27
19			AD26	AD25
20			AD24	CBE#3
21			AD22	AD23
22			AD20	AD21
23			AD18	AD19
24			PWRGDIN	REQ#3
25				
26			GND	GNT#3
27			AD16	AD17
28			FRAME#	IRDY#
29		VCC	CBE#2	DEVSEL#
30			TRDY#	LOCK#
31		GND	STOP#	PERR#
32				
33			GND	SERR#
34				AD15
35			CBE#1	AD14
36			PAR	AD12
37			GND	GND
38				
39			GND	M66EN
40			AD13	AD10
41			AD11	AD8
42			AD9	AD7
43			CBE#0	AD5
44			AD6	AD3

45			AD4	AD1
46			AD2	AD0
47				
48			VCC	VI/O
49			VCC	VCC
50		VCC	GND	GND
51			GND	GND
52		GND		

4 Board Parameters

4.1 Host Bus

100 MHz

4.2 PCI Local Bus

CPU to PCI Transfer Options:

Write post buffer

Max. 120 MByte/s (peak)

PCI to Memory Transfer Options:

Max. 120 MByte/s (peak)

Clock Speed:

33.3 MHz

IRQs:

Four PCI interrupts

4.3 Network

10BaseT/100BaseTx (twisted-pair)

Transfer Speed:

max. 10/100 Mbit/s

4.4 Serial I/O

2 Channels:

Full duplex, asynchronous

50 b/s - 115.2 Kbit/s

16 Byte Transmit and Receive FIFO

RS232 level

4.5 MTBF Values

Include one 64 MByte SODIMM:

81 774 h (computed after MIL HDBK-217E)

1 095 775 h (realistic value from industry stand experience)

4.6 ESD Values

2 kV (Human body method)

4.7 Environmental Conditions

Storage Temperature: -40° C - +70° C (non condensing)

Operating Temperature: 0° C - +55° C (1 m/s forced air cooling)

4.8 Maximum Operating Humidity:

85% relative

4.9 Power Requirements

Total Power Requirements (with one 64 MByte SODIMM, without PCI extensions):

4 A max. 1.8 A typ. +5 VDC +/-5%

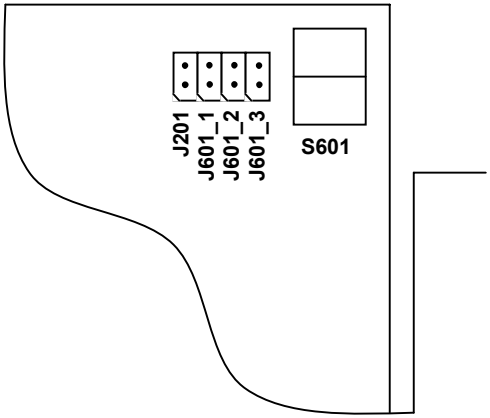
100 mA max. 30 mA typ. +12 VDC +/-10%

100 mA max. 10 mA typ. -12 VDC +/-10%

5 Jumpers

5.1 On-board Jumpers

Figure 5—1: Parts Side Jumpers



5.1.1 User-settable Jumpers

Table 5—1: Boot ROM Select (J601_1)

J601_1	Description
open	Boot from Boot-ROM (default)
Short	Boot from User-ROM (if present)

Table 5—2: External ROM Select (J601_2)

J601_2	Description
open	Boot ROM selected by J601_1 (default)
Short	Boot from external ROM (if present)

Table 5—3: External ROM Chipselect (J601_3)

J601_3	Description
	Used for chipselect of external ROM

Table 5—4: Revision-PROM Write-Protection (J201)

J1601	Description
Open	Revision-PROM is write protected
short	Revision-PROM is write enabled (default)

6 Appendix

6.1 Description of On-board Devices

This chapter describes how the on-board devices are accessed by operating system drivers. When an operating system, such as OS-9 and VxWorks, is used, there should be no need to address these devices with user-written code.

6.1.1 Memory Address Map

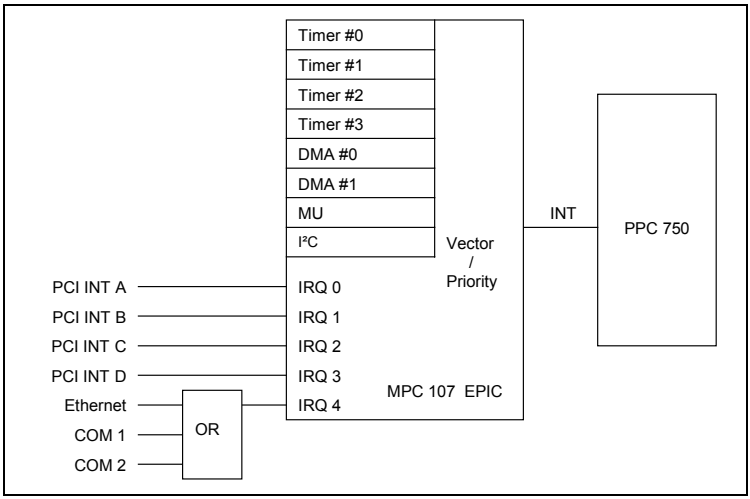
The BAB 911 uses address map B (CHRP) of the MPC107. After initialization the following address map becomes effective:

Table 6—1: Memory Address Map

CPU Address	PCI Address	Device
0000.0000-3FFF.FFFF	---	local RAM
4000.0000-77FF.FFFF	---	reserved
7800.0001	---	hex switch (bit 0-3, read only)
7800.0002	---	LED (bit 0-3, write only)
7800.0003-7BFF.EFFF	---	reserved
7BFF.F000-7BFF.FFFF	---	enable/retrigger watchdog
7C00.F001-7FFF.FFFF	---	reserved
8000.0000-FCDF.FFFF	8000.0000-FCDF.FFFF	PCI memory space
FCE0.0000-FCEF.FFFF	---	Embedded utilities memory block of MPC 107
FCF0.0000-FDFF.FFFF	FCF0.0000-FDFF.FFFF	PCI memory space
FE00.0000-FE00.FFFF	0000.0000-0000.FFFF	PCI/ISA I/O space
FE01.0000-FE7F.FFFF	0001.0000-007F.FFFF	reserved
FE80.0000-FEBF.FFFF	0080.0000-00BF.FFFF	PCI I/O space
FEC0.0000-FEDF.FFFF	CONFIG_ADDR	PCI configuration address register
FEE0.0000-FEEF.FFFF	CONFIG_DATA	PCI configuration data register
FEF0.0000-FF7F.FFFF	---	reserved
FF00.0000-FF3F.FFFF	---	non volatile RAM
FF40.0000-FF7F.FFFF	---	Dual UART
J601, pin 1-2 open pin 3-4 open:		
FF80.0000-FF9F.FFFF	---	optional Flash EEPROM
FFA0.0000-FFBF.FFFF	---	mirrored optional Flash EEPROM
FFC0.0000-FFC7.FFFF	---	System Flash EEPROM
FFC8.0000-FFFF.FFFF	---	mirrored System Flash EEPROM
J601, pin 1-2 short pin 3-4 open:		
Ff80.0000-FF87.FFFF	---	System Flash EEPROM
FF88.0000-FFBF.FFFF	---	mirrored System Flash EEPROM
FFC0.0000-FFDF.FFFF	---	optional Flash EEPROM
FFE0.0000-FFFF.FFFF	---	mirrored optional Flash EEPROM
J601, pin 1-2 open pin 3-4 short:		
FF80.0000-FF87.FFFF	---	System Flash EEPROM
FF88.0000-FFCF.FFFF	---	mirrored System Flash EEPROM
FFC0.0000-FFC7.FFFF	---	Emergency Flash EEPROM
FFC8.0000-FFFF.FFFF	---	mirrored Emergency Flash EEPROM

6.1.2 Interrupt Controller

Figure 6—1: BAB 911 Interrupt Diagram



This diagram shows how the on-board interrupt sources are connected to the interrupt controller, located in the MPC 107 chipset. This chip then prioritizes and drives the CPU interrupt input. The priority of the several interrupts is programmable by software.

6.1.3 Watchdog

The watchdog has a cycle time of typ. 1.6 sec. (1.0 ... 2.4 sec.). If not retriggered within this time the watchdog is generating a hardware reset.

After power on or hardware reset the watchdog is disabled. It will be enabled and a write cycle. Retriggering occurs by at least one write and one read cycle within the timeout period.

Table 6—2: Watchdog Address Assignment

Address	Description
$7BFFF000	first write cycle enables watchdog following read and write cycles retrigger watchdog

6.1.4 Configuration Switch

Table 6—3: Configuration Switch Address Assignment

Address	Description
$78000001	read byte: get hex value in the 4 LSBs, 4 MSBs are always "0" write byte: not allowed

6.1.5 Status Display

Figure 6—2: LEDs

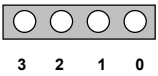


Table 6—4: Status Display Address Assignment

Address	Description
$78000002	read byte: reads undefined data write byte: the LEDs correspond to the 4 LSBs

6.1.6 Non Volatile RAM

Table 6—5: Non Volatile RAM Address Assignment

Address	Description
$FF000000 ... $FF007FFF	2 KByte of nvSRAM (only byte access allowed)

6.1.7 Serial Controller

The BAB 911 uses a ST16C2552 dual universal asynchronous receiver and transmitter (UART) which is clocked with 24 MHz. It is recommended to use the addresses $FF7FFFF0 to $FF7FFFF7 for serial channel #1 and $FF7FFFF8 to $FF7FFFFF for serial channel #2.

6.1.8 Soft Reset

The BAB 911 can be reset by writing bit 0 (observe byte ordering) of the Processor Initialization Register PI in the MPC 107 (at offset 0x41090 of the Embedded Utilities Memory Block). This will entirely reset the system.

6.1.9 Turbo Mode

As long as the Flash EPROMs are not accessed the BAB 911 can be operated in a turbo mode by setting the ROMFAL field in MCCR1 of the MPC 107 to 3. This halves the cycle times of the nvSRAM, serial controller, LED, configuration switch, and watchdog.

NOTES: